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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,946	12/20/2000	Steven W. Rogers	5150-52100	8700

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EXAMINER	
KE, PENG	

ART UNIT	PAPER NUMBER
2174	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,946	ROGERS ET AL.	
	Examiner	Art Unit	
	Peng Ke	2174	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to communications: Amendment, filed on 2/3/06.

This Action is mad FINAL.

Claims 1-52 are pending in this application. Claims 1, 10, 18, 26, 32, and 39 are independent claims.

Claim Rejections – 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 1-14, 16-29, and 31-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Teranishi et al. U.S. Patent 6,117,183.

As per claim 1, Teranishi e al teaches a method for propagating type information for hardware device nodes in a graphical program, wherein the method operates in a computer including a display screen and a user input device, the method comprising:

displaying on the display screen of the computer a first hardware device node in the graphical program in response to user input, wherein the graphical program comprises a plurality of interconnected nodes or icons, wherein the plurality of interconnected nodes or icons visually indicate functionality of the graphical program; (see Teranishi, column 7, lines 40-55)

associating the first hardware device node with a hardware device; (see Teranishi, column 7, lines 40-55)

displaying on the display screen a second hardware device node in the graphical program in response to user input; (see Teranishi, column 7, lines 40-55)

connecting the first hardware device node to the second hardware device node in response to user input; (see Teranishi, column 7, lines 40-55)

propagating information from the first hardware device node to the second hardware device node, wherein the information specifies the hardware device with which the first hardware device node is associated, wherein said propagating occurs in response to said connecting the first hardware device node to the second hardware device node; (see Teranishi, column 4, lines 5-26)

wherein the graphical program is executable by the computer. (see Teranishi, column 12, lines 20-41)

As per claim 2, which is dependent on claim 1, Teranishi teaches the method of claim 1. Teranishi further teaches wherein said displaying the first and second hardware device nodes in the graphical program comprises including the first and second hardware device nodes in a block diagram of the graphical program, wherein the block diagram visually indicates functionality of the graphical program. (see Teranishi, Figure 7, items L01-L04)

As per claim 3, which is dependent on claim 1, Teranishi teaches the method of claim 1. Teranisi further teaches comprising: associating the second hardware device node with the hardware device with which the first hardware device node is associated, in response to said propagating the information to the second hardware device node. (see Teranishi, column 4, lines 5-26)

As per claim 4, which is dependent on claim 1, Teranishi teaches the method of claim 1. Teranishi further teaches wherein said connecting the first hardware device node to the second hardware device node comprises connecting a wire from an output terminal of the first hardware device node to an input terminal of the second hardware device node. (see Teranishi, Figure 7, items L01-L04, column 7, lines 40-55; It is inherent that there must be an input terminal and an output terminal for the connection between L02 and L01)

As per claim 5, which is dependent on claim 1, Teranishi teaches the method of claim 1. Terranishi further teaches the method wherein said associating the first hardware device node with a hardware device comprises associating the first hardware device node with a hardware device class corresponding to the hardware device; wherein said propagating information from the first hardware device node to the second hardware device node comprises propagating information specifying the hardware device class with which the first hardware device node is associated. (see Teranishi, column 4, lines 5-26)

As per claim 6, which is dependent on claim 1. Teranishi teaches the method of claim 5. Terranishi further teaches the method comprising: associating the second hardware device node with the hardware device class, in response to said propagating the information to the second hardware device node. (see Teranishi, column 4, lines 5-26)

As per claim 7, which is dependent on claim 6. Teranishi teaches the method of claim 6. Terranishi further teaches the method comprising: associating the second hardware device node with a method of the hardware device class in response to user input; wherein during execution of the graphical program the second hardware device node is operable to invoke the method. (see Teranishi, column 4, lines 5-26, column 12, lines 20-41)

As per claim 8, which is dependent on claim 6, Terranishi teaches the method of claim 6. Terranishi further teaches the method comprising: associating the second hardware device node with a property of the hardware device class in response to user input; wherein during execution of the graphical program the second hardware device node is operable to perform one or more of: 1) getting the property; and 2) setting the property.(see Terranishi, column 4, lines 4-58)

As per claim 9, which is dependent on claim 1, Terranishi teaches the method of claim 1. Terranishi further teaches the method comprising: executing the graphical program, wherein during execution of the graphical program the second hardware device node is operable to access the hardware device. (see Terranishi, column 4, lines 58-column 5,lines 23)

As per claim 10, Teranshi teaches a method for performing type checking for a hardware device node in a graphical program, wherein the method operates in a computer including a display screen, the method comprising:

displaying on the display screen of the computer a first hardware device node in the graphical program in response to user input, wherein the graphical program comprises a plurality

of interconnected nodes or icons, wherein the plurality of interconnected nodes or icons visually indicate functionality of the graphical program; (see Teranishi, column 7, lines 40-55)

associating the first hardware device node with a first hardware device class in response to user input; (see Teranishi, column 7, lines 40-55)

selecting a method or property of the first hardware device class for the first hardware device node in response to user input; (see Teranishi, column 7, lines 40-55)

changing the first hardware device node to have an association with a second hardware device class in response to user input; (see Teranishi, column 4, lines 27-55)

and

performing type checking to determine whether the method or property is valid for the second hardware device class, in response to said changing the first hardware device node to have an association with the second hardware device class; (see Teranishi, column 5, lines 6-23)

wherein the graphical, program is executable by the computer. (see Teranishi, column 12, lines 20-41)

As per claim 11, which is dependent on claim 10. Teranshi teaches the method of claim 10. Teranshi further teaches the method comprising: indicating an invalid condition if the method or property is not valid for the second hardware device class. (see Teranshi, column 6, lines 58-column 7, lines 10)

As per claim 12, which is dependent on claim 11. Teranshi teaches the method of claim 11. Teranshi further teaches the method wherein said indicating the invalid condition comprises altering the visual appearance of a wire connected to an input terminal of the first hardware device node, wherein the wire provides information specifying the second hardware device class with which the first hardware device node is associated. (see Teranshi, column 6, lines 58-column 7, lines 10)

As per claim 13, which is dependent on claim 11. Teranshi teaches the method of claim 10. Teranshi further teaches method comprising:

preventing execution of the graphical program if the method or property is not valid for the second hardware device class. (see Teranshi, column 8, lines 30-35)

As per claim 14, which is dependent on claim 11. Teranshi teaches the method of claim 10. Teranshi further teaches the method wherein the first hardware device node has an input terminal for receiving information specifying a hardware device class with which to associate the first hardware device node; (see Teranishi, column 4, lines 27-55)

wherein said associating the first hardware device node with the first hardware device class comprises connecting a first wire to the input terminal; (see Teranishi, column 4, lines 27-55)

wherein said changing the first hardware device node to have an association with a second hardware device class comprises connecting a second wire to the input terminal. (see Teranishi, column 4, lines 27-55)

As per claim 16, which is dependent on claim 10. Teranshi teaches the method of claim 10. Teranshi further teaches the method wherein said performing type checking to determine whether the method or property is valid for the second hardware device class comprises: determining a list of valid methods and properties for the second hardware device class; and

determining whether the method or property is included in the list of valid method and properties. (see Teranshi, column 6, lines 58-column 7, lines 10)

As per claim 17, which is dependent on claim 16. Teranshi teaches the method of claim 16. Teranshi further teaches the method wherein said determining the list of valid methods and properties for the second hardware device class comprises determining the valid methods and

properties from a type library, wherein the type library includes information regarding the second hardware device class. (see Teranshi, column 7, lines 26-40)

As per claim 18, it is rejected with same rationale as claim 1. (see rejection above)

As per claim 19, which is dependent on claim 18, it is of the same scope as claim 2. (see rejection above)

As per claim 20, which is dependent on claim 18, it is of the same scope as claim 3. (see rejection above)

As per claim 21, which is dependent on claim 18, it is of the same scope as claim 4. (see rejection above)

As per claim 22, which is dependent on claim 18, it is of the same scope as claim 5. (see rejection above)

As per claim 23, which is dependent on claim 22, it is of the same scope as claim 6. (see rejection above)

As per claim 24, which is dependent on clam 23, it is of the same scope as claim 7. (see rejection above)

As per claim 25, which is dependent on claim 23, it is of the same scope as claim 8. (see rejection above)

As per claim 26, it is rejected with the same rationale as claim 10. (see rejection above)

As per claim 27, which is dependent on claim 26, it is of the same scope as claim 11. (see rejection above)

As per claim 28, which is dependent on claim 26, it is of the same scope as claim 13. (see rejection above)

As per claim 29, which is dependent on claim 26, it is of the same scope as claim 14. (see rejection above)

As per claim 31, which is dependent on claim 26, it is of the same scope as claim 16. (see rejection above)

As per claim 32, it is rejected with same rationale as claim 1. (see rejection above)

As per claim 33, which is dependent on claim 32, it is of the same scope as claim 2. (see rejection above)

As per claim 34, which is dependent on claim 32, it is of the same scope as claim 3. (see rejection above)

As per claim 35, which is dependent on claim 32, it is of the same scope as claim 5. (see rejection above)

As per claim 36, which is dependent on claim 35. Teranshi teaches the system of claim 35. Teranshi further teaches the system processor is further operable to execute program instructions stored in the memory to associate the second hardware device node with the hardware device class, in response to said propagating the information to the second hardware device node. (see Teranishi, column 4, lines 27-55)

As per claim 37, which is dependent on claim 36, it is of the same scope as claim 7. (see rejection above)

As per claim 38, which is dependent on claim 36, it is of the same scope as claim 8. (see rejection above)

As per claim 39, it is rejected with same rationale as claim 10. (see rejection above)

As per claim 40, which is dependent on claim 39, it is of the same scope as claim 16. (see rejection above)

As per claim 41, which is dependent on claim 39, Teranishi teaches the claim 39. Teranishi further teaches the graphical program is interpretable or compliable to generate instructions executable by the computer. (see Teranishi, column 12, lines 20-41)

As per claim 42, which is dependent on claim 39, Teranishi teaches the claim 39. Teranishi further teaches the graphical program comprises a dataflow diagram. (figure 3, items a-c)

As per claim 43, which is dependent on claim 32, it is of the same scope as claim 41. (see rejection above)

As per claim 44, which is dependent on claim 32, it is of the same scope as claim 42. (see rejection above)

As per claim 45, which is dependent on claim 26, it is of the same scope as claim 41. (see rejection above)

As per claim 46, which is dependent on claim 26, it is of the same scope as claim 42. (see rejection above)

As per claim 47, which is dependent on claim 18, it is of the same scope as claim 41. (see rejection above)

As per claim 48, which is dependent on claim 18, it is of the same scope as claim 42. (see rejection above)

As per claim 49, which is dependent on claim 10, it is of the same scope as claim 41. (see rejection above)

As per claim 50, which is dependent on claim 10, it is of the same scope as claim 42. (see rejection above)

As per claim 51, which is dependent on claim 1, it is of the same scope as claim 41. (see rejection above)

As per claim 52, which is dependent on claim 1, it is of the same scope as claim 42. (see rejection above)

Claim Rejections – 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Teranishi et al. U.S. Patent 6,117,183 further in view of McKaskle et al. US Patent 5,481,741.

As per claim 15, Teranishi teaches the method of claim 10. However he fails to teach the method wherein the first hardware device node is a register access node.

McKaskle et al. teaches a wherein the first hardware device node is a register access node. (figure 100 a-d)

It would have been obvious to an artisan at the time of the invention to include McKaskle's teaching with method of Teranishi in order to allow users to simulate a control register.

As per claim 30, which is dependent on claim 26, it is of the same scope as claim 15. (see rejection above)

Response to Argument

Applicant's arguments filed on 2/3/06 have been fully considered but they are not persuasive.

Applicant's arguments focused on the following:

1) Teranishi fails to teach a graphical program.

2) Ternaishi fails to teach propagating information from a fist hardware device node to a second hardware device node, where the information specifies the hardware device with which the first hardware device node is associated.

Examiner disagrees.

1) The examiner does not agree for the following reasons:

During patent examination, the pending claims must be "given >their< broadest reasonable interpretation consistent with the specification." > In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

In this case, Teranishi teaches a graphical program because Teranishi discloses a graphical user interface that allows user to move, update, and associate virtual objects. (column 4, lines 51-68)

2) Ternaishi teaches this limitation because Teranishi locates the problematic sign path within a circuit. (column 4, lines 1-25) In order the locate the problematic path, Teranishi simulates the circuit (column 6, lines 17-30) and its components and that requires propagating information from one hardware device node to another device. (column 6, lines 46-58, column 8, lines 12-53)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peng Ke whose telephone number is (571) 272-4062. The examiner can normally be reached on M-Th and Alternate Fridays 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine L. Kincaid can be reached on (571) 272-4063. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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